AMENDMENT TO CLAIMS

In the Claims

Please **AMEND** claims 1, 3, and 4.

A copy of all pending claims and a status of the claims are provided below.

1. (Currently Amended) A thin film transistor array panel, comprising:

an insulating substrate;

a gate line formed on the substrate;

a plurality of storage electrodes formed on the substrate, each storage electrode including a plurality of branches, wherein one of the branches has an isolated end and the remaining branches form a closed loop, and wherein the isolated end is electrically connected by a connector to a storage electrode line formed on the substrate;

a gate insulating layer formed on the gate line and the storage electrode;

a semiconductor layer formed on the gate insulating layer;

a data conductor formed on the semiconductor layer;

a passivation layer formed on the data conductor; and

a pixel electrode layer formed on the passivation layer~~,~~

~~wherein at most one of the branches of each storage electrode has an isolated end~~.

2. (Previously Presented) The thin film transistor array panel of claim 1, wherein adjacent storage electrodes are connected by connecting portions.

3. (Currently Amended) The thin film transistor array panel of claim 1, wherein the connector is ~~further comprising~~ a connection bridge having a portion thereof connected to ~~each of~~ the isolated end[[s]] of each of the plurality of storage electrodes and a portion thereof connected to [[a]] the storage electrode line formed on the substrate.

4. (Currently Amended) The thin film transistor array panel of claim 1, wherein the plurality of branches of each storage electrode further comprises two longitudinal branches [[and]] connected to two oblique branches[[, and]] to form the ~~branches of each storage conductor form a~~ closed loop.

5. (Previously Presented) The thin film transistor array panel of claim 1, wherein each storage electrode comprises two longitudinal branches connected to three oblique branches, the connected branches forming two closed loops.

6. (Previously Presented) The thin film transistor array panel of claim 1, wherein each storage electrode comprises two longitudinal branches connected to four oblique branches, the connected branches forming three closed loops.

7. (Previously Presented) The thin film transistor array panel of claim 1, wherein the pixel electrode has a plurality of cutouts, and at least one of the cutouts overlaps the storage electrode.

8. (Previously Presented) The thin film transistor panel of claim 1, wherein the data conductor has substantially the same planar shape as the semiconductor layer except for a channel portion of the semiconductor layer.

9. (Previously Presented) A thin film transistor array panel, comprising:

an insulating substrate;

a gate line formed on the substrate;

a plurality of storage electrodes formed on the substrate, each storage electrode including a plurality of branches;

a gate insulating layer formed on the gate line and the storage electrode;

a semiconductor layer formed on the gate insulating layer;

a data conductor formed on the semiconductor layer;

a passivation layer formed on the data conductor; and

a pixel electrode layer formed on the passivation layer,

wherein at most one of the branches of each storage electrode has an isolated end, and

wherein longitudinal portions of adjacent storage electrodes are connected by connecting portions.

10. (Previously Presented) The thin film transistor array panel of claim 9, further comprising a connection bridge having a portion thereof connected to each of the isolated ends of the plurality of storage electrodes and a portion thereof connected to a storage electrode line formed on the substrate.

11. (Previously Presented) The thin film transistor array panel of claim 9, wherein each storage electrode further comprises two longitudinal branches and two oblique branches, and the branches of each storage conductor form a closed loop.

12. (Previously Presented) The thin film transistor array panel of claim 9, wherein each storage electrode comprises two longitudinal branches connected to three oblique branches, the connected branches forming two closed loops.

13. (Previously Presented) The thin film transistor array panel of claim 9, wherein each storage electrode comprises two longitudinal branches connected to four oblique branches, the connected branches forming three closed loops.

14. (Previously Presented) The thin film transistor array panel of claim 9, wherein the pixel electrode has a plurality of cutouts, and at least one of the cutouts overlaps the storage electrode.

15. (Previously Presented) The thin film transistor array panel of claim 9, wherein the data conductor has substantially the same planar shape as the semiconductor layer except for a channel portion of the semiconductor layer.